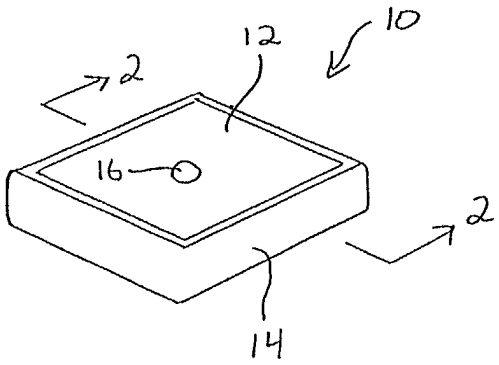

FIG. 1

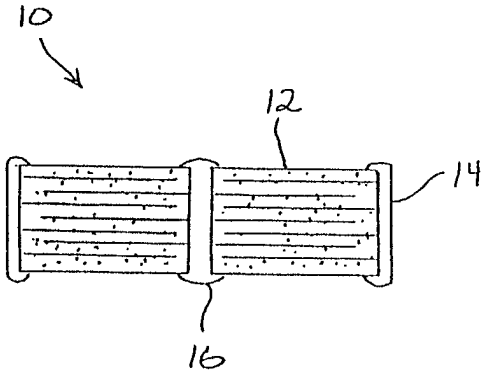

FIG. 2

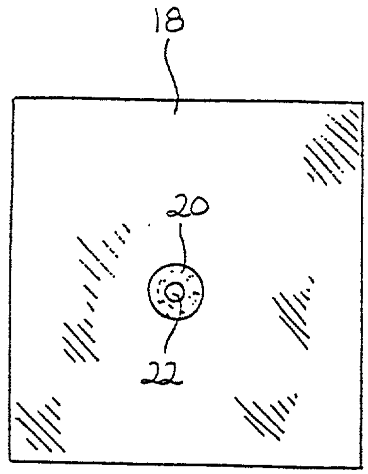

FIG. 3A

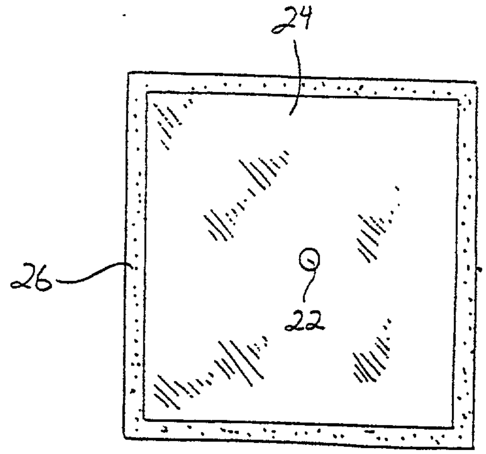

FIG. 3B

e.g. VIA LAYOUT FOR CONTACTS FOR MICROPROCESSOR

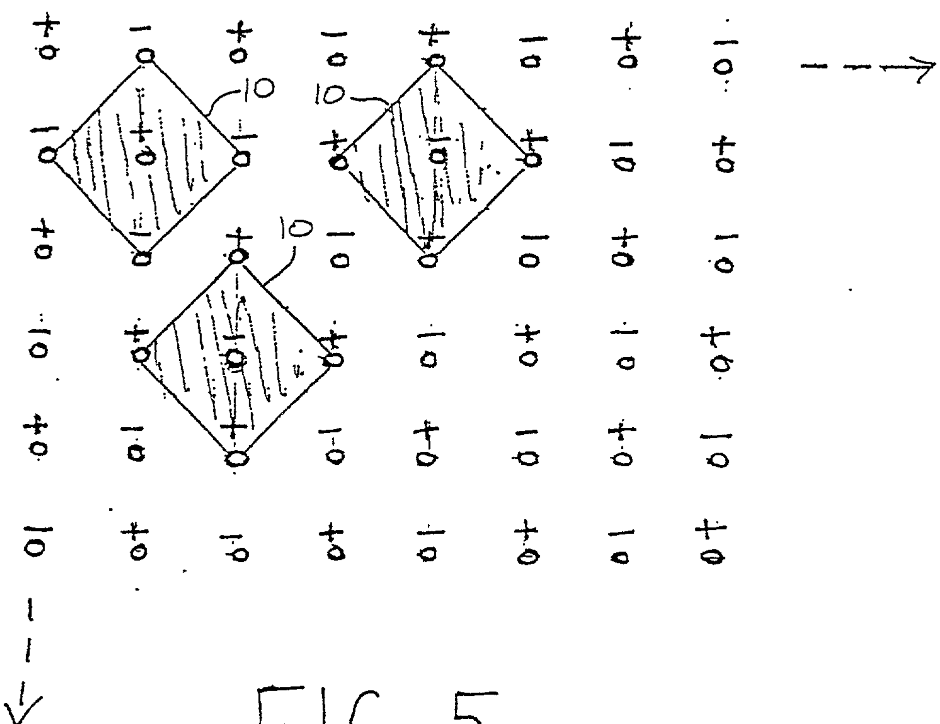

FIG. 5

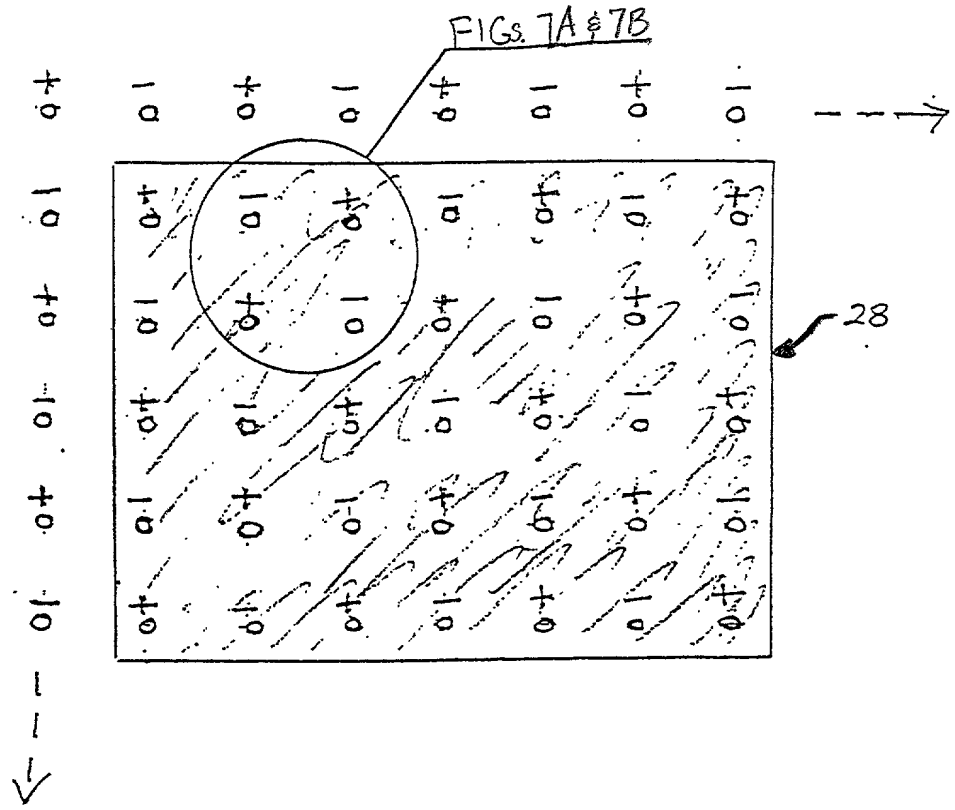

FIG. 6

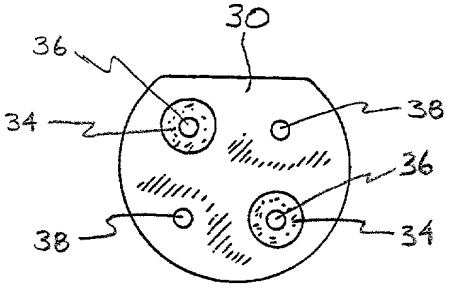

FIG. 7A

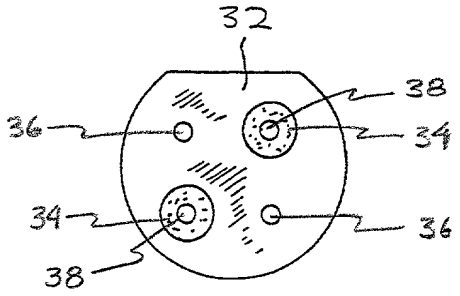

FIG. 7B